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ALUSGDI: Low power arithmetic logic unit based sliced processor using GDI and MGDI

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ABSTRACT

In recent years, many digital logic circuits in terms of transistors such as Pass Transistor Logic (PTL), Complementary Metal Oxide Semiconductor (CMOS) logic and etc. have been used for implementing DSP algorithms. Gated Diffusion Input (GDI) logic is also another method for implementing digital circuits. In this work, GDI logic style is used in the proposed ALU based Filter Bank. The ALU unit of the proposed filter bank is designed by modified GDI logic. Power consumption of the entire design is also reasonably reduced using recursive parallel self-timed adder. GDI logic has three terminals which are Common Gate (G), PMOS (P)/NMOS (N) and output terminal. The number of transistors is reduced when compared to Complementary Metal Oxide Semiconductor (CMOS) logic. Hence, the reduced number of transistors eliminates the switching activity and power dissipation. The GDI logic consumes 65% less area and 91.4% less power when compared to CMOS logic. The modified GDI logic provides 77.5% area reduction when compared to CMOS logic. The experimental results obtained using the proposed ALU based Sliced Processor by employing GDI logic compared with the traditional filter bank techniques. ALU based filter bank design speeds up significantly through GDI concepts when compared to the interpolated filter bank and the design is implemented in 65 nm CMOS technology.

1. Introduction

VLSI circuits are mainly classified into (i) Programmable Logic Devices (PLD) and (ii) Non-programmable Application Specific Integrated Circuits (ASIC). Signal processing algorithms are implemented in a proficient fashion using Field Programmable Gate Array (FPGA) platform. Generally, Digital Signal Processing applications are implemented in general purpose signal processing chips for audio applications, special purpose filtering chips and ASIC [6]. FPGAs are advantageous over traditional ASIC, due to its programmability and flexibility. FPGA was invented in 1985, primarily to enable higher integration, higher performance and increased flexibility. High integration depends on the number of transistors used in the circuit. Various logic styles are used for the implementation of digital circuits. Modified Gate Diffusion Input logic consumes less power when compared to Gated Diffusion Input (GDI) logic design and CMOS logic design. In the Modified GDI logic circuit designs the Analysis such as DC and Transient are calculated for a wider range logic cell. Practical implementations expose the modified GDI is advantageous over GDI and CMOS in common factors such as power, delay and area [1,2]. It permits to obtain speed, low power consumption and area of the design. The comparisons based on the number of devices that is being used, delay of the circuit and power leakage. Various digital logic circuits using several logic styles were designed and analyzed their properties with simulation results. Minimization of power in CMOS circuit is described. An adder was implemented with 8-bit input using m GDI. The design includes full adders, ripple carry adder and a carry look ahead adder. The architecture was implemented in 180 nm technology to maintain minimum delay, area and low power. In Ref. [3], booth multiplier and carry look ahead adder is used to design a FIR filter to make the circuit faster. Basic primitive cells have been designed in Refs. [4,5] using mGDI.

Fig. 1 shows the combinations of input and output with various

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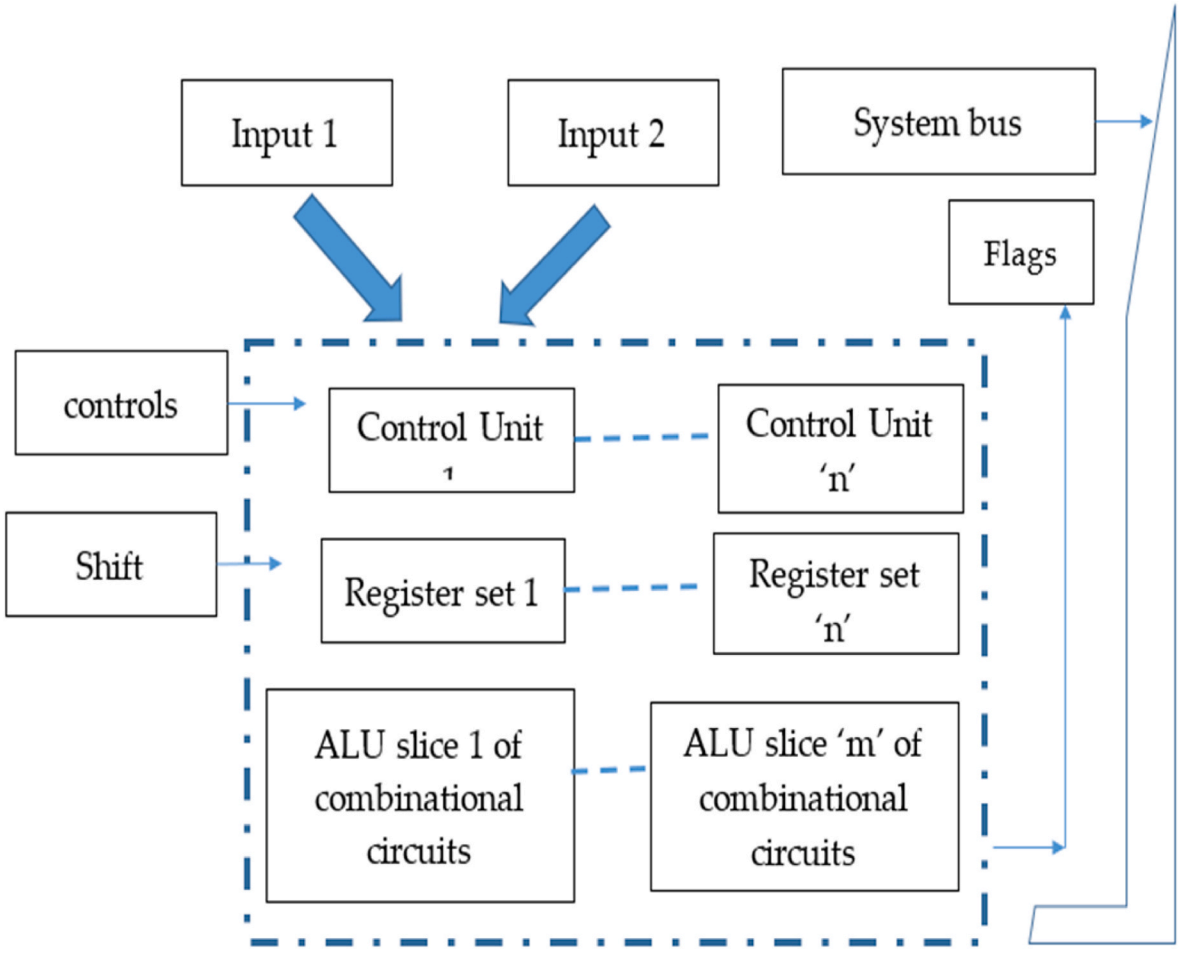


Fig. 1. Block Diagram of ALU based Sliced Preprocessor.

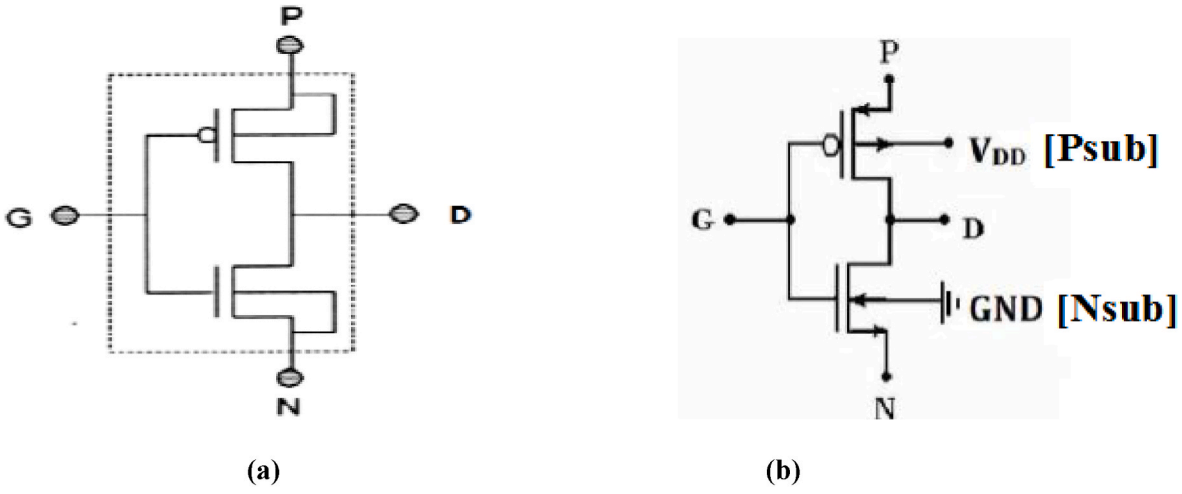


Fig. 2. (a) Basic GDI cell (b) modified GDI cell.

control units to perform the operations. ALU sliced into many blocks that are implemented using GDI and mGDI logic as mentioned below.

1.1. GDI

Gated Diffusion Input (GDI) logic [6,7] same as an inverter design but it has important differences.

Terminals associated to Gated Diffusion Input (GDI) as inputs are common terminal for n-type and p-type transistors (i) Gate (G) (ii) Source/Drain input to PMOS (iii) source/drain input NMOS as shown in Fig. 2 (a). Connection established from Bulk PMOS to P and NMOS bulk to N.

1.2. Modified GDI

Modified GDI technique [6] includes PMOS terminal of substrate

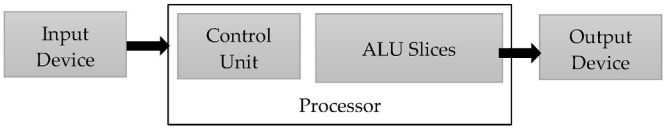


Fig. 3. Block diagram of ALU

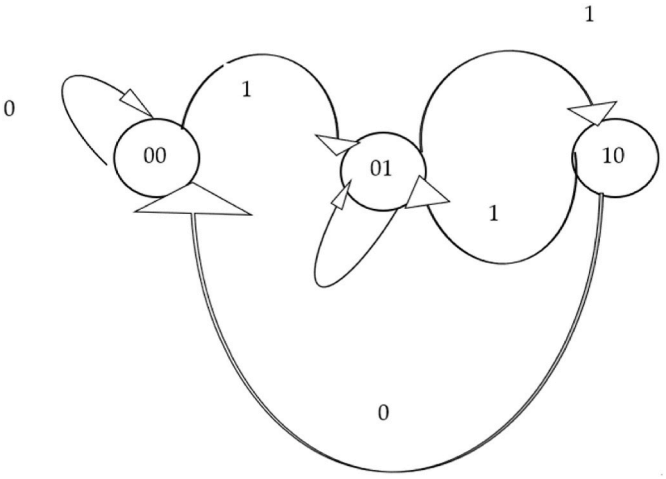


Fig. 4. State Diagram- Iterative structures.

Table 1
Comparisons based on Delay and Power for the Proposed Circuits.

Gates	Inputs	Delay (ps)	Power (μW)	PDP (aJ)
XOR	2 input	26.1	0.25	17.59
	3-input	23.6	0.377	29.39
	proposed	21.9	13.36	156.31
AND	2 input	25.8	2.50	64.5
	3-input	25.6	2.47	63.2
	proposed	21.5	2.46	52.9
MUX	2 input	121.2	0.25	30.3
	4-input	134.9	0.35	47.21
	proposed	13.58	10.41	141.37
PASTA	16T	123.9	0.53	65.66
	19T	136.3	0.84	114.45
	proposed	15.91	20.7	329.55
MAC	16T	125.2	0.71	226.1
	19T	122.4	0.69	218.6
	proposed	131.5	0.68	223.4

Table 2
FPGA results.

Description	Buffers	Hexa-core	Quad-core
Slices used	298	224	224
No. of LUTs	276	241	241
Frequency in MHz	263	256	256

(Psub) which is given to the VDD and substrate of NMOS (Nsub) is attached to GND which is shown in Fig. 2(b). Therefore, Modified GDI cell is configured through existing CMOS technologies. Table III shows several logic operations which can realize with the help of modified GDI.

This proposed work expands based on the investigations of the literature, by considering the following.

- ➢ The proposed method focuses on the proposed ALU based Sliced Processor using GDI
- ➢ Area of circuit can be diminished using modified GDI logic.

Table 3
Implementation results.

Methods	Clock cycle	Maximum Frequency in MHz	Maximum Throughput per sec	Hardware area (in no. of transistors)
Proposed	1	710	0.73	195
ALUSGDI	2	467	0.93	210
Filter bank	3	318	0.95	234
	4	243	0.97	335
Filter bank	1	710	0.11	228
with GDI	2	467	0.43	237
logic	3	318	0.52	258
	4	243	0.80	362
Filter bank	1	710	0.22	231
with CMOS	2	467	0.54	274
logic	3	318	0.67	282
	4	243	0.91	367

Table 4
Performance comparisons.

Parameters	CMOS	GDI	MODIFIED GDI
Bits processed	3.45	3.39	4.85
Frequency	512	500	221
Delay (ns)	1.76	1.53	1.32
Area (no. of transistor count)	142	52	31
Throughput	1.96	2.11	1.23
Power	1.87 mW	2.8 mW	1.392 nW

- ➢ Power consumption is also reasonably reduced based on the strategies used in the method.
- ➢ Delay of the proposed method is decreased in the ALU processor unit.

The paper organized as follows. Section 2 explains about the Materials and methods of the proposed method. Section 3 presents the results. Section 3 describes about the conclusion.

2. Materials and methods

Fig. 3 shows the block diagram of ALU with control and memory units. First memory is used as Read Only Memory (ROM) and next memory is to accumulate input values in Random Access Memory (RAM). This block performs various operations and computations of input values which represent in 2's complement form. Many filter bank algorithms are discussed in Refs. [8,9]. The parallel self-timed adder consists of multiplexers, half adder for minimal number of interconnections. It also contains completion detection unit which is used to detect the completion of the process. In Multiplexer design, half adder is designed using gate diffusion input logic. When selection line is zero, multiplexer selects one input using the control signal and fed those inputs to half adder which produces sum and carry. When the selection line is one, multiplexer selects another input and the process continues until all the carry becomes zero. XOR gate is designed using GDI logic [10,11]. The DSP algorithm works under iterative structure of state diagram shown in Fig. 4. The multiplexer block is enabled in the iterative mode when the select signal is ON. The recursive structure is executed number of times for each and every transition. Totally three states 00, 01 and 10. In each state, multiple transitions take place, as stated in the diagram. Gate delays are represented to distinct the specific state.

Filter banks are divided into many parts depends on various aspects such as complexity of circuit, power and area. The proposed filter structure includes an accumulation unit which is connected with a multiplier and an addition/subtraction unit which helps to proficiently perform the Multiply-Accumulate (MAC) operation [12–15]. This paper proposes an ALU based circuit. ALU is important for many DSP Applications. MAC unit of any circuit decides the delay and significance of operation. Multiplication-and-accumulate functions are crucial part in

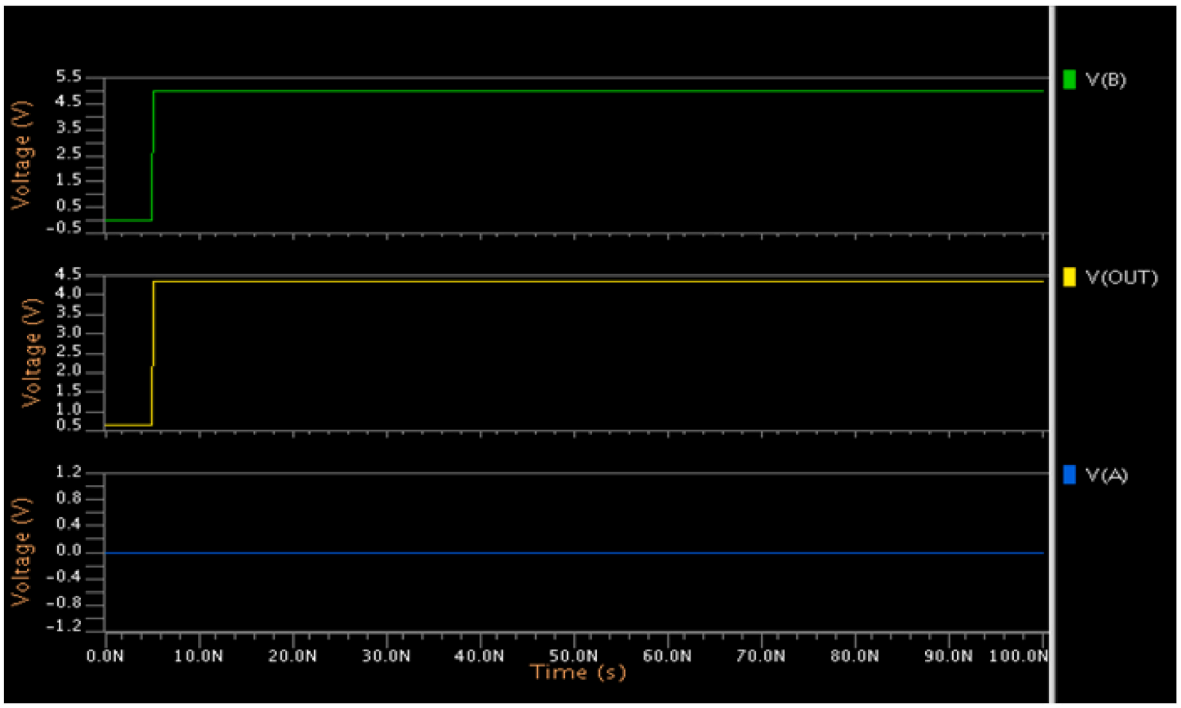


Fig. 5. Simulation Results XOR gate using Modified GDI logic.

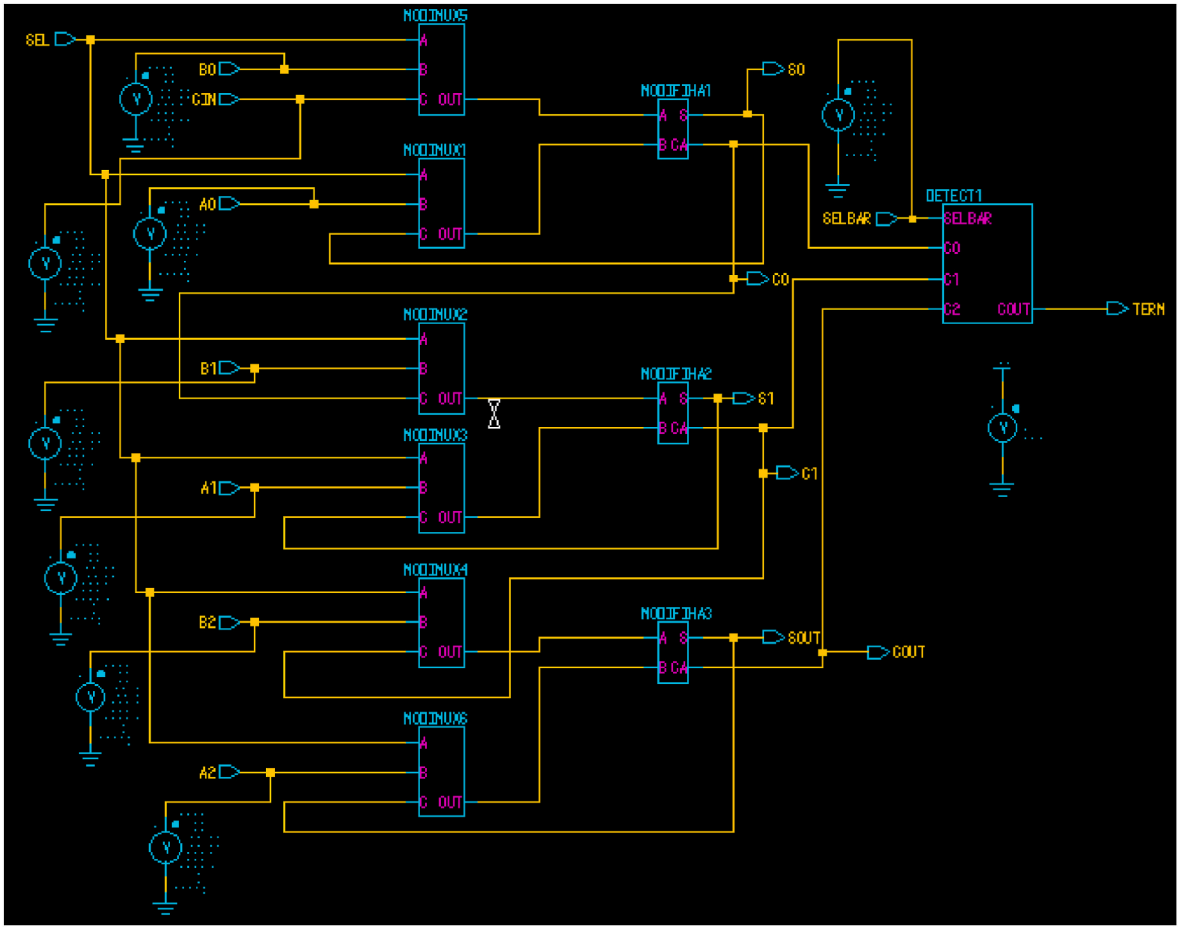


Fig. 6. mGDI-PASTA.

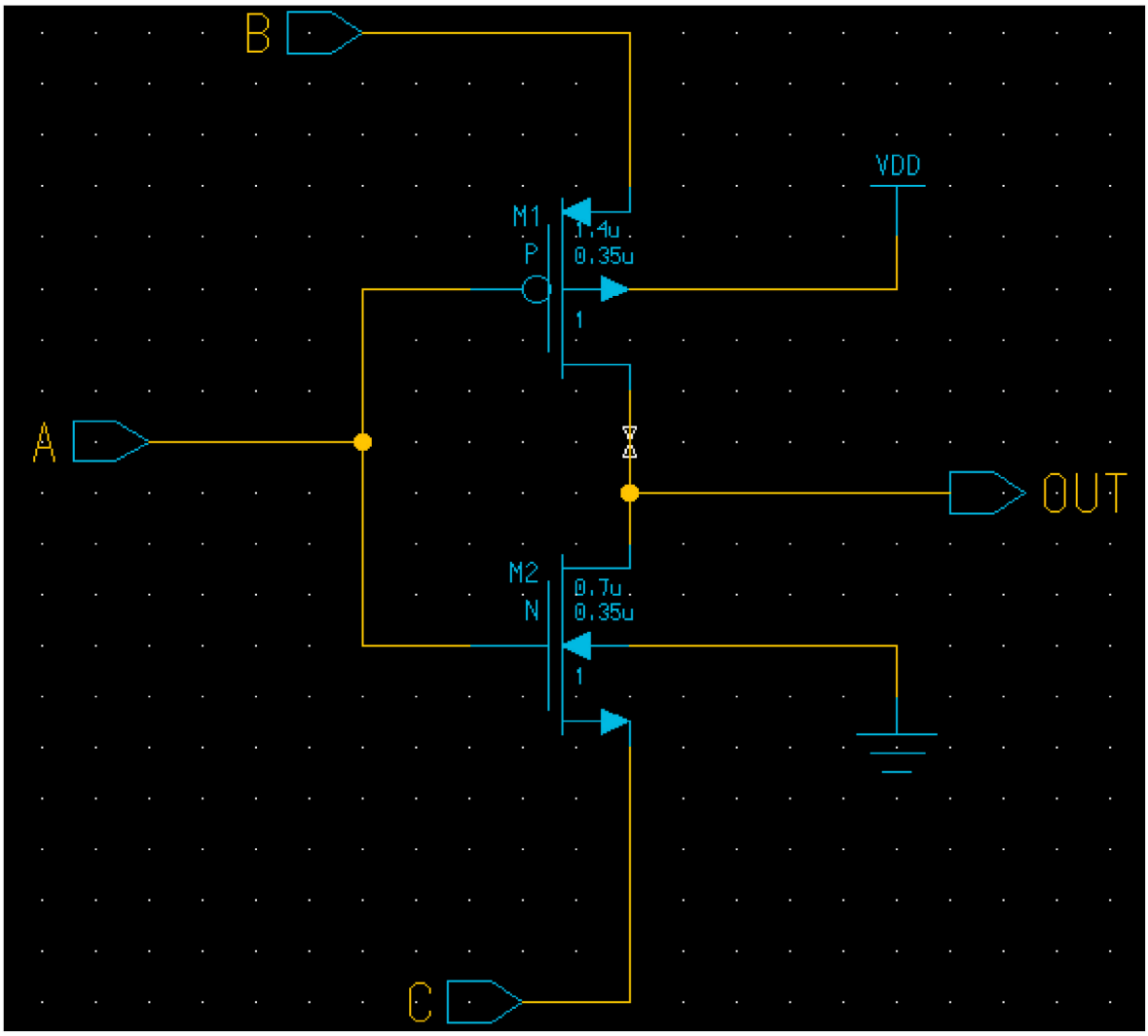


Fig. 7. mGDI Multiplexer.

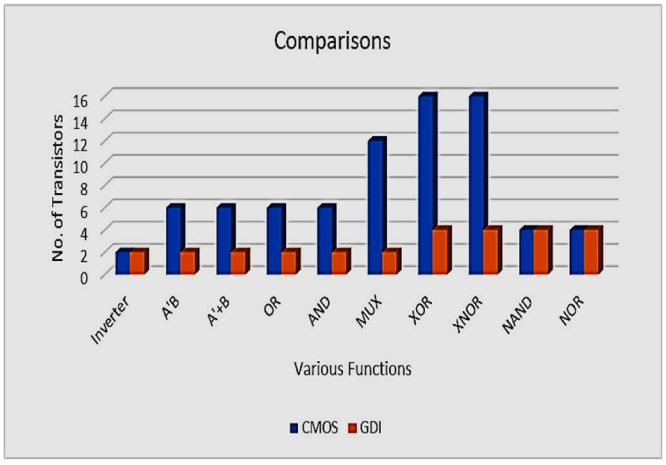


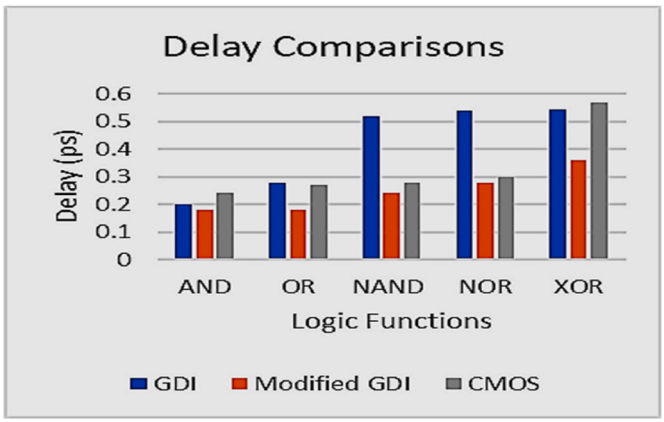
Fig. 8. GDI vs. CMOS: Comparison based on Number of Transistors.

digital filter designs [16–18]. Hence, the performance of ALU block allows low delay with filter process. Meanwhile, the ALU block performs entirely self-regulating of the Computer Processing Unit (CPU), which fixes the data independently and hence reduces the CPU load. The multiply accumulate unit includes multiplication, addition and an accumulation register to store the output [19–21]. The ALU block is shown in Fig. 6. This proposed method can be implemented for hearing aid devices.

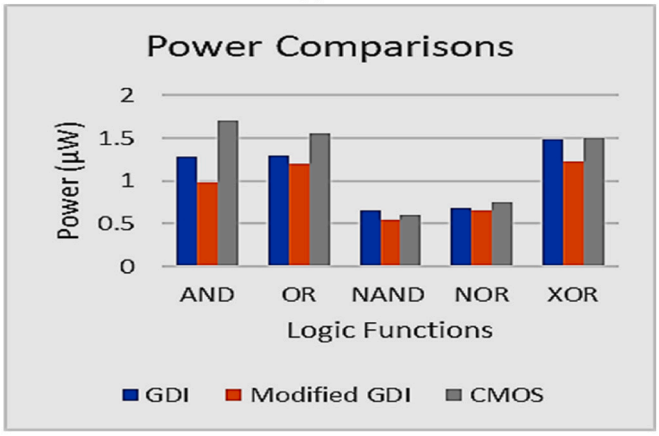
3. Results

The inputs are simultaneously given to the circuit in which the control units are performed the operations as the control input is enabled. ALU slice 1 of combinational circuits are implemented for both GDI and mGDI logic to diminish the power consumption. The multiplexer in each and every stage selects the appropriate operation of the ALU processor. It states the relation between the components used in the circuit and explains about the aspect ratio of each and every transistor. In 8-bit ALU, A0, A1, A2, A3, A4, A5, A6, A7 are taken as the input samples for the simulations. Based on the control input the arithmetical and logical or relational operations can be performed.

It is observed that how a processor can append computations effectively to accommodate the upcoming inputs using the control unit. The MAC unit of the proposed technique is also implemented in GDI. Multiplexer using GDI and mGDI are also stated in the simulation results. The scale of transistors has been chosen for ideal PDP using the measuring technique in the proposed transistor and values are stated in Table 1. By and by, the driving capacity in the devices is debased which is based on the parasitic capacitances and resistances amid the



(a)



(b)

Fig. 9. Comparison based on Power (a) and Delay (b) using GDI, Modified GDI and CMOS Logic.

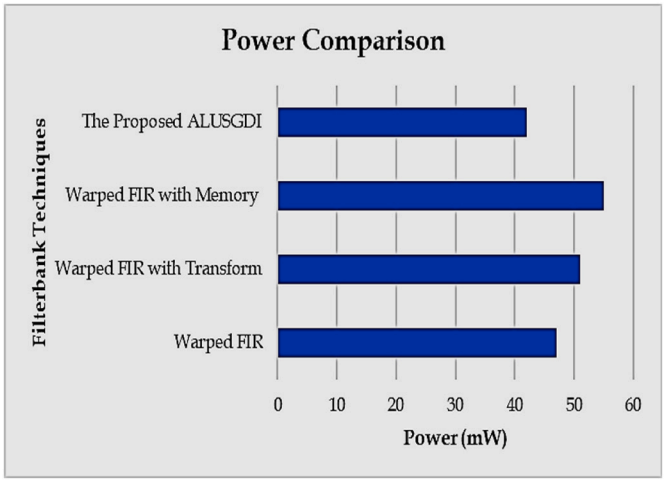


Fig. 10. Comparison based on Power.

development, and transistors voltage over the time, yet the output enhances this circumstance.

There are XOR, AND, one 2-1-MUX, PASTA and MAC circuits using contributions of the circuit and furthermore diminish the obstruction from the VDD and GND. An altered technique to the transistor measurement for innovative design is proposed. Emerging strategy which helps numerical calculation by choosing the proper size of transistors on a circuit and furthermore it holds accuracy and high speed, what's more,

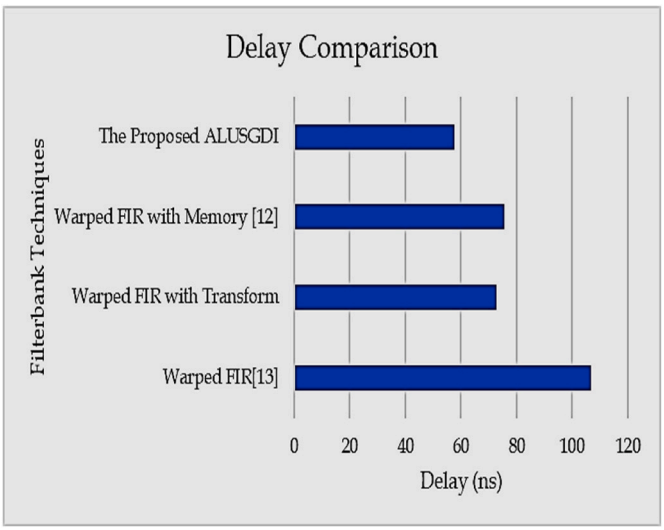


Fig. 11. Comparison based on Delay.

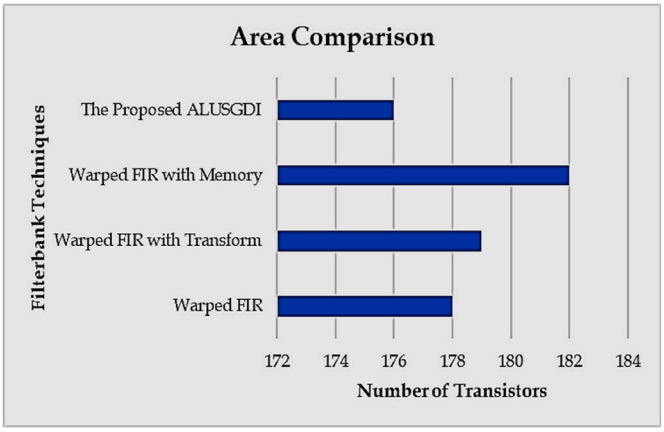


Fig. 12. Comparison based on Area.

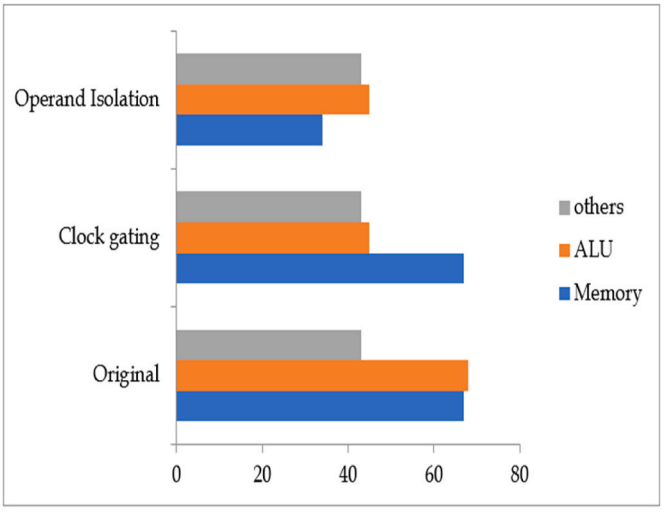


Fig. 13. Component utilization in different modes.

joining. Moreover, developing various blocks of the design, results shown that the proposed circuits have a decent execution in every single reenacted condition. Power consumption is reduced by utilizing the

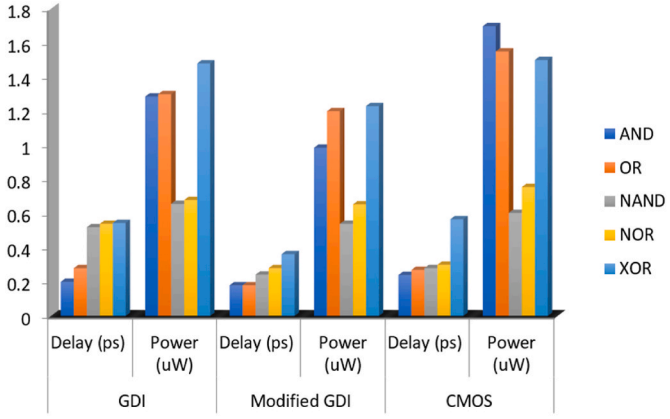


Fig. 14. Overall Comparison of logical functions.

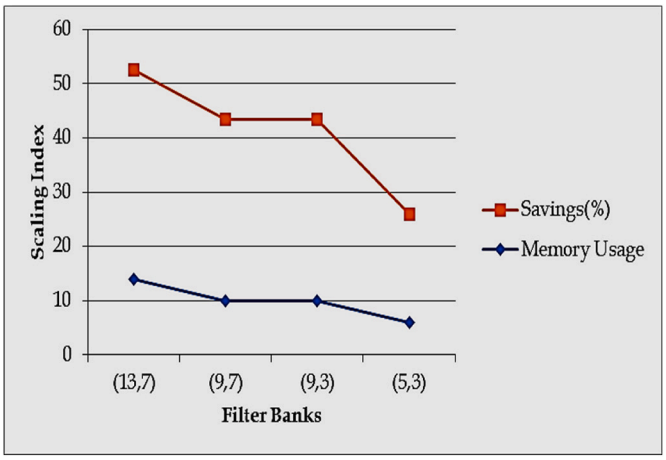


Fig. 15. Performance Metrics based on scaling index.

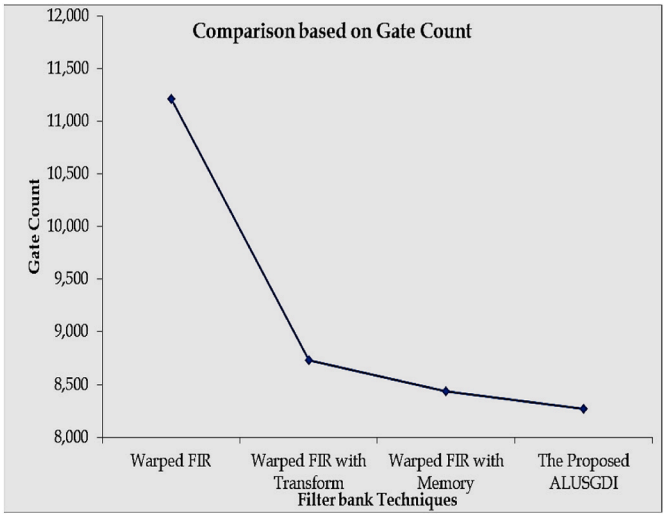


Fig. 16. Area comparison in terms of gate count.

mGDI structure. And the delay is modeled in the circuit with minimum load and less cut-off.

There is a power reduction of 7.2% accomplished, as the drive strength is changing from 13 mA to 10 mA at the frequency of 11 MHz, 3.3V. 5.6% of reduction achieved in power where the drive strength drops from 8 mA to 6 mA at 15 MHz, 2.5 V. XOR gate holds the power of

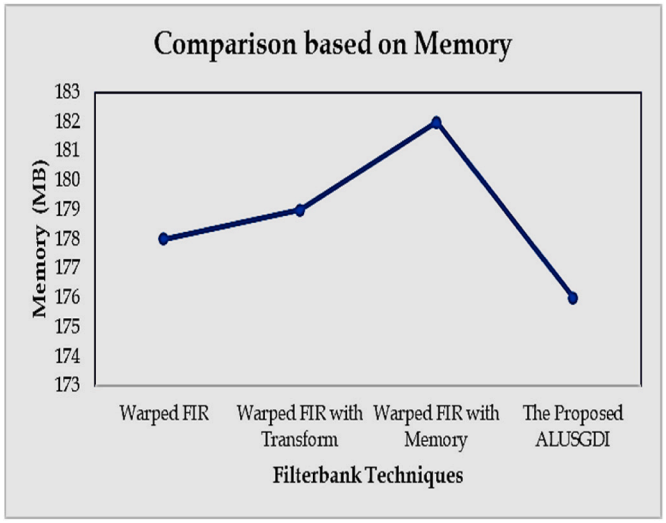


Fig. 17. Performance Metrics in terms of memory.

13.36 μW and 156.31 aJ as PDP. PASTA and MAC both are achieved significantly reduced power, delay and power delay product when compared to 16 T and 19T. In the proposed MUX block, reasonable reduction of 131ps in delay, 10.41 μW in power and 141.37 aJ in power delay product are attained. MUX was implemented in 65 nm CMOS technology, 3.3 V, 50 MHz environment.

Table 2 shows the FPGA results. It is implemented in multicores such as hexa-core and quad-core. The number of slices used for the complete design and the number of LUTs along with its frequency are stated in the FPGA results for buffers, hexa-core and quad-core. It provides better solutions for balancing the load.

Table 3 shows the implementation results for a number of clock cycle for the filter bank with various logic styles. The number of clock cycle executed here is 4. In each clock cycle, the maximum frequency, maximum throughput is recorded. Hardware area is analyzed with the transistor counts in every clock cycle. The performance comparisons of the proposed ALU, based on various parameters such as number of processed bits, delay, area, throughput, power and frequency are shown in Table 4 for the CMOS, GDI and mGDI.

Fig. 5 states the simulation results of XOR gate using mGDI. The simulation result shows two inputs V(A) and V(B). When both the inputs are low, the output is low. In the second input V(A) is low and V(B) is high so its output is high. Fig. 6 shows the schematic diagram of PASTA using mGDI. PASTA consists of an adder and a MUX. When sel is '0', the feedback path from the adder establishes the consecutive iterations to proceed up till the signals will assume '0' values.

Fig. 7 shows the schematic diagram of MUX using mGDI. The terminals Vdd and Gnd are connected in the PMOS bulk and NMOS bulk respectively. Input A is commonly applied to control terminal of both gates. NMOS source terminal is applied to C which is the select signal. Input B is given to the PMOS terminal. The operation of the MUX decides based on the selection line. If C = '1', the input A is selected and if C = '0', the input B is selected. The desired output can be achieved by varying the input samples.

The schematic diagram of 8-bit ALU design by using Modified GDI logic. These operations can be done using an XOR gate, Multiplexer and PASTA with minimum number of transistors i.e., mGDI logic. The arithmetic operations are accomplished in terms of the selection signal. Entire circuit shows minimum average power when the process length is reduced. This results PASTA to consume less power. The performance of the design is further optimized by the pull-down transistors. Fig. 8 states that GDI vs. CMOS: Comparison based on Number of Transistors. CMOS logic gets a greater number of logic gates than GDI. Fig. 9 (a) shows the delay comparison of the logic functions. Fig. 9 (b) states the power

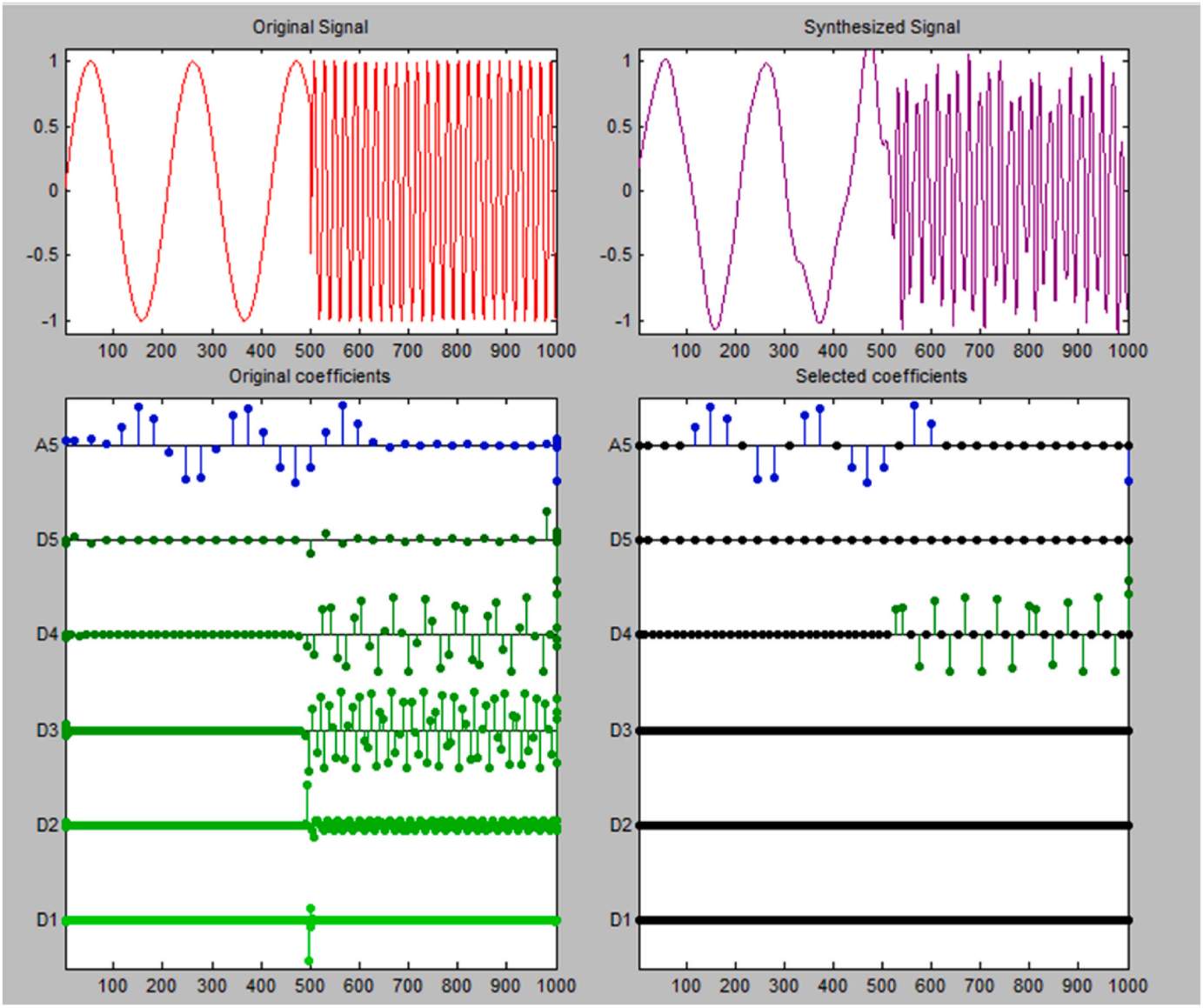


Fig. 18. Implementation -ALUSGDI

comparison of the logical functions. The results obtained are comparatively modified GDI gets reasonable output.

Fig. 10 Comparisons based on power, delay and area are carried out for the proposed method using mGDI logic and the results are obtained as follows. Fig. 11 shows comparison based on power and Fig. 12 shows the delay comparison for filter bank techniques. The Proposed ALUSGDI achieves low power and minimum power than other filter bank techniques.

Fig. 11. Comparison based on Area.

Fig. 12 shows the Area comparison in terms of number of transistors used for filter bank techniques. The Proposed ALUSGDI achieves minimum area comparatively than other filter bank techniques. Fig. 13 states the utilization such as Memory, ALU and other components of sliced processor in different modes like original, clock gating and operand isolation. Operand isolation method is used to reduce power by suppressing the redundant operations in a circuit and reduces the unwanted switching in the circuit. Clock gating is a technique which is used to reduce power dissipation.

Fig. 14 shows overall comparison of logical functions such as AND, OR, NAND, NOR and XOR. Fig. 15 states the performance metrics based on scaling index and memory savings for different filter bank coefficients.

Fig. 16 describes the area comparison in terms of gate count. Fig. 17 states the performance metrics based on memory usage. The comparison describes that the proposed method consumes minimum area when compared to the warped FIR, warped FIR with Transform and warped FIR with memory. Fig. 18 describes the implementation of the proposed ALUSGDI.

4. Conclusions

ALU based processor unit is proposed using modified GDI logic. Every circuit element in the proposed method were implemented by applying the recursive parallel self-timed adder. The delay and power consumption for two architectures were found and the analysis report was generated using Xilinx. In this proposed method, adaptive circuits for MAC with synchronous ability introduced. In this paper, circuits are exceedingly upgraded the power utilization with minimum delay, which causes less cut off. All circuits of the proposed method have its own advantages with respect to delay, driving capacity, control utilization, Power Delay Product (PDP). The proposed method states the technology specific power delay optimization. 65-nm CMOS process demonstrates,

and proves that the proposed method over other logics have predominant minimum power consumption and delay. In the future work, the ALU unit design can be suggested using other logics such as pass transistor logic and adiabatic logic. Techniques such as clock gating, multiple Vdd can be implemented to reduce circuit complexity even better. The GDI logic occupies 65% area reduction and 91.4% minimum power when compared to CMOS logic. The modified GDI logic provides 77.5% less area when compared to CMOS logic. The proposed method has an disadvantage when implementing GDI, bulk terminal connections became problem.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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